018403

August/September 2022

B.Tech. (CSE(AIML)/CE/CSE/IT) IV SEMESTER

Computer Organization and Architecture (PCC-CS-402)

Time : 3 Hours] [Max. Marks : 75

Instructions :

1. *It is compulsory to answer all the questions (1.5 marks each) of Part-A in short.*
2. *Answer any four questions from Part-B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

PART-A

1. (a) Explain the stored program concept in computer. (1.5)

   (b) Distinguish between Computer Organization and Computer Architecture. (1.5)

   (c) What is a hardwired control unit? (1.5)

   (d) Distinguish between remainder restoring and non-restoring division algorithm. (1.5)

   (e) What is the need of memory hierarchy in computer system? (1.5)

(f) Compare programmed I/O and interrupt initiated I/O. (1.5)

(g) Write the advantage of write through cache policy. (1.5)

(h) Discuss the basic concept of pipelining. (1.5)

(i) How interleaved memory is used in 8086 micro-processor? (1.5)

(j) What is the need of concurrent access of memory in parallel processors? (1.5)

PART-B

2. (a) Draw and explain the flow chart of integer addition and subtraction of binary numbers. (10)

(b) Why addressing modes are used in computer systems? Explain. (5)

3. (a) What is a flag register in 8086 microprocessor? Explain. (5)

(b) Represent the decimal number - 307.1875 in single precision and double precision floating point format. (10)

4. What is a micro programmed control unit? Explain the microinstruction and address sequencing. (15)

5. (a) Multiply $(-9) \times (-13)$ using Booth's Multiplication algorithm. (5)

(b) Why I/O interface is used? Explain the working of DMA. (10)

6. (a) Explain the cache coherence problems with solution in parallel processors. (10)

(b) What is asynchronous data transfer? Explain the priority interrupt. (5)

7. (a) A computer uses 32-bit byte addressing. The computer uses a 2-way set associative cache with a capacity of 32 kB. Each cache block contains 16 bytes. Calculate the number of bits in the TAG, SET and OFFSET fields of a memory address. (5)

(b) Differentiate between overlapped and non-overlapped execution by using space time diagram. Also explain the different 5 stages of pipeline. (10)